Introduction

Zilker Labs' power management and conversion ICs are synchronous voltage-mode buck converters based on the patented Digital-DC™ technology. The buck converter is used to convert a higher, often loosely regulated voltage to a lower, tightly regulated voltage. The buck converter uses a MOSFET in the "freewheeling" or bottom switch location to increase efficiency. The operation of a buck converter is illustrated in Figure 1.

General Circuit Description

The buck converter shown in Figure 1 is a well- known switching power supply topology. It operates by turning on and off the control MOSFET (QH) at a high frequency. The amount of time the QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by the following equation where T_{on} is time on and T_{sw} is the switching period.

$$D = \frac{T_{on}}{T_{sw}} \qquad \textbf{Eq. [1]}$$

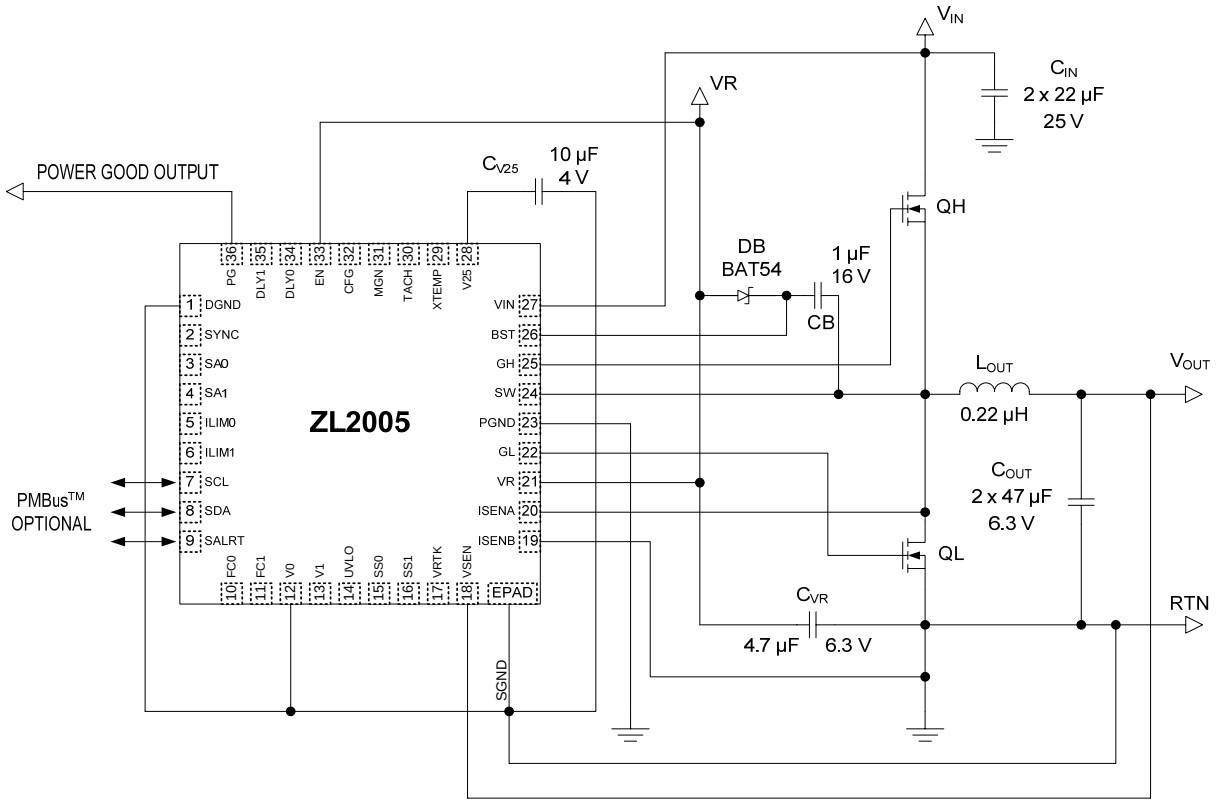

Figure 1. Typical Application Circuit

To simplify the analysis of this circuit, assume the following:

- Input voltage value (V_{IN}) is constant
- Output voltage value (V_{OUT}) is constant
- Average inductor current is not decreasing or increasing

Under these assumptions, the net voltage across the inductor during a switching period must equal zero. This can be described by the following equations:

$$D(V_{IN} - V_{OUT}) = (1 - D) \times V_{OUT} \quad \textbf{Eq. [2]}$$

$$D = \frac{V_{OUT}}{V_{IN}} \quad \textbf{Eq. [3]}$$

During D, QH is on and V_{IN}–V_{OUT} is applied across the inductor. The current ramps up as shown in Figure 2.

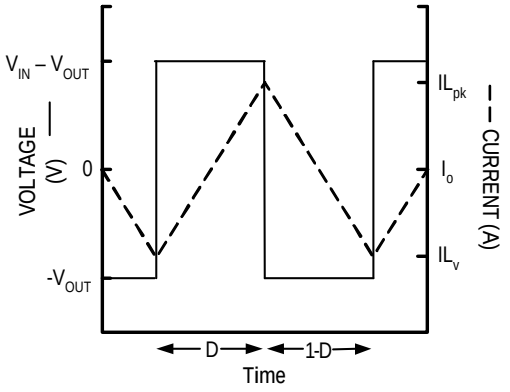

Figure 2. Inductor Waveforms

When the top MOSFET turns off, the current flowing in the inductor must continue to flow from the ground up through the synchronous MOSFET (QL), after which the current ramps down. The output capacitor C_{OUT} is selected with a low impedance at the switching frequency so the AC component of the inductor current is filtered from the output voltage and the load sees a nearly DC voltage.

The input capacitor C_{IN} is likewise sized to source the AC component of the current flowing through the top MOSFET to prevent this AC current from being drawn from elsewhere in the system.

Buck Power Stage Losses

Each component in the power stage of the buck converter dissipates power. The input and output capacitors dissipate power in their equivalent series resistances (ESR) proportional to the ripple current flowing through them. The inductor dissipates power in its ESR and in core material loss.

Core loss is proportional to the ripple current flowing through the inductor and the frequency of the ripple. The synchronous MOSFET dissipates power in two ways: in its channel resistance (R_{DSON}) as a function of current and in the gate drive current needed to turn the MOSFET on and off.

The gate drive current loss is proportional to frequency. Likewise, the control MOSFET also dissipates power in its R_{DSON} and gate drive current as well as in its turn-on and turn-off transitions.

The power dissipated in these transitions, called switching loss, is proportional to frequency. Because many of the power stage component losses are proportional to frequency, increasing frequency increases power loss and thus lowers efficiency.

Buck Converter LC Filter

The LC filter smoothes the chopped input voltage generated by QH and QL to provide a low noise DC output voltage. The size of this filter is inversely proportional to the switching frequency. The inductor core loss also increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency.

To select the appropriate power stage components for the desired performance goals, the power supply requirements listed in Table 1 must be known.

Table 1. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0–14.0 V	12 V
Output voltage (V_{OUT})	0.6–5.0	1.2 V
Output current (I_{OUT})	0 to ~30 A	20 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output step load	< I_o	50% of I_o
Output step load rate	—	10 A/µS
Step load deviation	—	50 mV
Maximum PCB temp.	120°C	85°C
Desired efficiency	—	85%
Desired size	—	Optimize for small size

Design Goal Trade-offs

The design of the buck power stage requires several compromises among size, efficiency, and cost. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a frequency based on Table 2. This frequency is a starting point and may be adjusted as the design progresses.

Table 2. Design Considerations by Frequency

Frequency Range	Design Considerations
200 – 400 kHz	High efficiency, larger size
400 – 800 kHz	Moderate efficiency, smaller size
800 kHz – 2 MHz	Lower efficiency, smallest size

Inductor Selection

When selecting an output inductor, several trade-offs must be considered. Inductance must be sufficient to generate a low ripple current (I_{opp}). Low ripple current will allow smaller output capacitance to be used while still achieving the desired output ripple voltage.

Because high inductance values compromise output transient load performance, a balance must be struck between low ripple current that allows low output ripple and high ripple current that allows a small output deviation during transient load steps. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \qquad \textbf{Eq. [4]}$$

Now the output inductance can be calculated using the following equation, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}} \qquad \textbf{Eq. [5]}$$

The average inductor current is equal to the maximum output current. The peak inductor current is calculated using the following equation where I_{OUT} is the maximum output current:

$$IL_{pk} = I_{OUT} + \frac{I_{opp}}{2} \qquad \textbf{Eq. [6]}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above. Table 3 lists suggested inductor vendors and series.

Table 3. Suggested Inductors

Vendor	Series	Output Current
Wurth	WE-HC	Up to 30 A
Coiltronics	HC8	Up to 30 A
Vishay	IHLP5050	Up to 30 A
Vishay	IHLP2525	Up to 10 A

Saturation characteristic also should be considered when selecting an output inductor. Saturation is the reduction of the effective inductance of the inductor as the current through it increases.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. In such conditions, an inductor that still provides some inductance to protect the load and the power supply MOSFETs from damaging currents is desirable. Consequently, gapped ferrite inductors are not recommended because of their rapid drop in inductance in over-current conditions. The inductors in Table 3 are distributed gap cores that will provide some inductance in over-current conditions.

Once an inductor is selected, the ESR and core losses in the inductor are calculated. Use the ESR specified in the inductor manufacturer's datasheet:

$$Power = ESR \times IL_{rms} \qquad \textbf{Eq. [6]}$$

IL_{rms} is given by

$$IL_{rms} = \sqrt{I_{OUT}{}^2 + \frac{(I_{opp}/2)^2}{3}} \qquad \textbf{Eq. [7]}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

Output Capacitor Selection

Several trade-offs also must be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, those capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output voltage ripple voltage to the capacitor ESR and the other half to capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8fs * V_{OUT} * V_{orip}/2} \qquad \textbf{Eq. [8]}$$

$$ESR = \frac{V_{OUT} * V_{orip}/2}{I_{opp}} \qquad \textbf{Eq. [9]}$$

Use these values to make an initial capacitor selection. Some sample capacitor types are listed in Table 4. Select a single capacitor or parallel several capacitors to meet the ESR and capacitance requirement. Ceramic capacitors provide the lowest ESR and are the smallest size, but have relatively small capacitance values.

Organic semiconductor capacitors, also known as OS-CON capacitors, have relatively low ESR with relatively large capacitance values, but are larger than ceramics and have more series inductance, which can degrade their performance. Tantalum capacitors have greater ESR, but with larger capacitance values than ceramics. Tantalum capacitors must be surge-tested for use in power supplies. After a capacitor has been selected, the resulting output voltage ripple can be calculated using

$$V_{orip} = I_{opp} * ESR + \frac{I_{opp}}{8fs * C_{OUT}} \qquad \textbf{Eq. [10]}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

The performance of the power supply in response to a transient load is quantified by

$$V_{ostep} = I_{ostep} * \frac{2t_{nlr} + tl_{out}}{2C_{OUT}} + 0.02 * V_{OUT} \quad \textbf{Eq. [11]}$$

where tl_{out} represents the time needed to ramp the current in the output inductor, as given by

$$tl_{out} = \frac{I_{ostep} * L_{OUT}}{V_{INM} - V_{OUT}} \quad \textbf{Eq. [12]}$$

and where t_{nlr} is the delay of the non-linear response circuit expressed as

$$t_{nlr} = 1/16fs \quad \textbf{Eq. [13]}$$

These equations highlight the ZL2005's non-linear response (NLR) circuit. The NLR allows the ZL2005 to respond quickly to a load transient to minimize the amount of output capacitance needed.

Regardless of the type of output capacitors selected, the NLR will be activated when the output deviates 2% from the desired output voltage. Once activated, the NLR bypasses the pulse width modulator in the ZL2005 and immediately alters the duty cycle to correct for the output deviation.

The capacitors selected should be checked against the NLR equations. If the step response specification is met by a large margin, the inductor ripple current can be lowered by increasing the value of the inductor and thus lowering the output capacitance required. Conversely, if the step response requirement is not met, either the frequency or the inductor ripple current must be increased.

MOSFET Operation in a Synchronous Buck Converter

The on-time of the control MOSFET QH sets the conversion ratio from the input voltage to the output voltage. When QH is off, the inductor current continues to flow in the synchronous MOSFET QL.

To avoid a short circuit across the input voltage supply, the ZL2005 must ensure that QH and QL are not on at the same time. When QH and QL are both on, the condition is called *cross conduction*. When both QH and QL are off, the condition is called *dead time*.

During the dead time, the inductor current must flow in the parasitic drain diode in QL. The voltage drop and the resulting power loss in this diode are greater than what would occur if the current were flowing in the drain of QL. Therefore, the dead time should be minimized, but not to the extent that the MOSFETs cross-conduct.

The ZL2005 incorporates a unique algorithm that continuously optimizes the MOSFET dead time based on the efficiency of the power stage. Even with optimized dead time, there is always some delay between when either QH or QL is turned off and QH or QL is turned on. As a result, QL is always turned on and off with current flowing in the drain diode.

Because the voltage across the drain diode is smaller than the supply input voltage, QL is turned on and off with very little loss. QH, however, is turned off and on with nearly the full input supply voltage applied from its drain to its source. Therefore, QH experiences losses both when it is turned on and turned off.

Table 4. Suggested Capacitors

Type	Vendor	Series	Capacitance	ESR
Ceramic	TDK	C3216X5R	47 µF	2.5 mΩ
Organic Semiconductor	Vishay	255D	220 µF	40 mΩ
Tantalum	Vishay	593D	100 µF	100 mΩ

QL Selection

The bottom MOSFET should be selected primarily based on the device's R_{DSON} and secondarily based on its gate charge. To choose QL, use the following equation and allow 2–5% of the output power to be dissipated in the R_{DSON} of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$PQL = (0.02 \sim 0.05) \times V_{OUT} \times I_{OUT} \quad \textbf{Eq. [14]}$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = \sqrt{\frac{(1-D)}{3} * (3{I_{OUT}}^2 + \frac{1}{4}{I_{opp}}^2)} \quad \textbf{Eq. [15]}$$

Calculate the desired R_{DSON} as follows:

$$R_{DSON} = PQL / {I_{botrms}}^2 \quad \textbf{Eq. [16]}$$

Note that the R_{DSON} given in the manufacturer's datasheet is measured at 25°C. The actual R_{DSON} in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of 125°C has an R_{DSON} 1.4X higher than the value at 25°C.

Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = fs * Q_g \quad \textbf{Eq. [17]}$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80 mA.

MOSFETs with lower R_{DSON}s tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are contained in the ZL2005, this power is dissipated in the ZL2005 according to the following equation:

$$Power = fs * Q_g * V_{IN} \quad \textbf{Eq. [18]}$$

QH Selection

In addition to the R_{DSON} loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2–5% of the output power to be dissipated in the R_{DSON} of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = \sqrt{\frac{D}{3} * (3{I_{OUT}}^2 + \frac{1}{4}{I_{opp}}^2)} \quad \textbf{Eq. [19]}$$

Calculate a starting R_{DSON} as follows:

$$PQH = (0.02 \sim 0.05) \times V_{OUT} \times I_{OUT} \quad \textbf{Eq. [20]}$$

$$R_{DSON} = PQH / {I_{toprms}}^2 \quad \textbf{Eq. [21]}$$

Select a candidate MOSFET, and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80 mA.

Next, calculate the switching time using

$$t_{sw} = \frac{V_{INM} * C_{gd}}{I_{gdr}} \quad \textbf{Eq. [22]}$$

where C_{gd} is the gate to drain capacitance of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2005.

Although the ZL2005 has a typical gate drive current of 4 A, use the minimum guaranteed current of 2 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using

$$P_{swtop} = V_{INM} * t_{sw} * I_{OUT} * fs \quad \textbf{Eq. [23]}$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad \textbf{Eq. [24]}$$

MOSFET Thermal Check

Once the power dissipations for QH and QL have been calculated, the MOSFETs junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$Tj\max = T_{pcb} + P_Q * R_{th} \quad \textbf{Eq. [25]}$$

For further details of thermal analysis and design see Zilker Labs Application Note 10 [1].

Several examples of MOSFETs that can be used for QH and QL are listed in

Table 5. MOSFETS for QH and QL

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Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V “bulk” supply from an off-line, computer-grade power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple can be determined from the following equation, where η is the converter efficiency, usually around 90%:

$$I_{rms} = I_{OUT} * \sqrt{\left(\frac{V_{OUT}}{V_{INM}}\right)\left[1+\left(\frac{V_{OUT}}{V_{INM}}\right)\left(\frac{1-2\eta}{\eta^2}\right)\right]}$$

Eq. [26]

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. Furthermore, filter capacitors on the input bus may not be rated to handle this much ripple current, and heating of these devices could lead to premature failure.

The input capacitors should be rated at 1.4X the ripple current calculated above to assure a 50% power derating. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

CB Selection

This capacitor is the filter for the bootstrap bias voltage that is used to drive the top MOSFET. It should be large enough to minimize voltage drop while providing drive current between charging pulses as a function of the drop and gate charge of the top FET. This is done by sizing CB such that the charge needed to turn on the top MOSFET is less than 1/100 the charge stored in CB. Using the gate charge specified in the MOSFET manufacturer’s datasheet and the relationship Q = C × V,

$$CB = \frac{100Q_g}{4.5\ \text{V}}$$

Eq. [27]

Table 5. MOSFETS for QH and QL

Part Number	Mfg	R_{DSON} (mΩ)	V_{DS}	Q_g (nC)	Case
IRF6609	IR	2.6	20	46	MT
IRF6620	IR	3.6	20	28	MX
IRF6637	Vishay	7.7	20	11	MP
IRF6617	IR	8.1	20	11	ST
SUD70N02_03P	Vishay	5.3	20	40	DPAK
IRF7834	IR	5.5	20	29	SO8
Si7106DN	Vishay	6.2	20	18	PP1212
Si7406DH	Vishay	65	20	5	SC70-6
Si5404DC	Vishay	30	20	12	S1206-8
Si2312DS	Vishay	31	20	8	SOT23
Si6404DQ	Vishay	10	30	32	TSSOP8
NTMFS4108N	ON	3.2	30	47	PPSO8

As an example, a 10 nC MOSFET would need CB = 0.2 µF. CB should be a stable dielectric such as X7R and rated 6.3 V or more.

CV25 Selection

This capacitor is used to both stabilize and provide noise filtering for the 2.5 V internal power supply. It should be between 4.7 and 10 µF, should use a semi-stable X5R or X7R dielectric ceramic with a low (less than 10 mΩ) ESR, and should have a rating of 4 V or more.

CVR Selection

This capacitor is used to both stabilize and provide noise filtering for the 5 V reference supply (V_R). It should be between 2.2 and 10 µF, be a semi-stable X5R or X7R dielectric ceramic capacitor with a low ESR less than 10 mΩ, and be rated 6.3 V or more. Because the current for the bootstrap supply is drawn from this capacitor, CVR should be sized at least 10X the value of CB so that a discharged CB does not cause the voltage on it to drop excessively during a CB recharge pulse.

DB Selection

This Schottky diode is used to provide the bootstrap voltage. The bootstrap voltage is a floating bias supply used to drive the top MOSFET. It can be any Schottky diode rated for 200 mA average, 500 mA peak, with less than a 0.5 V forward drop and reverse voltage rating of at least 30 V. The BAT54C in the SOT23 or SC75 package is recommended. The anodes of this device can be connected together as shown in Figure 1.

References

[1] AN2010 – *ZL2005 Thermal and Layout Guidelines*, Zilker Labs, Inc., 2005.

Revision History

Date	Rev. #	
9/30/05	0.8	Initial release
9/25/06	1.0	Changed Eq. [22], Eq. [26], and CV25 Selection
5/01/09	AN2011.0	Assigned file number AN2011 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to application note content.

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